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| 10/634,337 | 08/04/2003 | Bo-Yong Chung | 50432/P849 | 6765 |

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| EXAMINER |
|---|
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**Please find below and/or attached an Office communication concerning this application or proceeding.**

The time period for reply, if any, is set in the attached communication.

-- *The MAILING DATE of this communication appears on the cover sheet with the correspondence address* --

**Period for Reply**

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE <u>3</u> MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.
- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

**Status**

1)☒ Responsive to communication(s) filed on <u>02 April 2007</u>.

2a)☒ This action is **FINAL**.     2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

**Disposition of Claims**

4)☒ Claim(s) <u>1-28,31-34,36 and 37</u> is/are pending in the application.

    4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☒ Claim(s) <u>9,10,12-14,24,26,31-34,36 and 37</u> is/are allowed.

6)☒ Claim(s) <u>1-8,11,15-23,25,27 and 28</u> is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

**Application Papers**

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on <u>04 August 2003</u> is/are: a)☒ accepted or b)☐ objected to by the Examiner.

    Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

    Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

**Priority under 35 U.S.C. § 119**

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

    a)☐ All  b)☐ Some * c)☐ None of:

      1.☐ Certified copies of the priority documents have been received.

      2.☐ Certified copies of the priority documents have been received in Application No. _____.

      3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

    * See the attached detailed Office action for a list of the certified copies not received.

**Attachment(s)**

1)☐ Notice of References Cited (PTO-892)

2)☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)

3)☒ Information Disclosure Statement(s) (PTO/SB/08)
    Paper No(s)/Mail Date <u>4/2/2007</u>.

4)☐ Interview Summary (PTO-413)
    Paper No(s)/Mail Date. _____.

5)☐ Notice of Informal Patent Application

6)☐ Other: _____.

# DETAILED ACTION

## Claim Rejections - 35 USC § 103

1.      The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all

obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set
> forth in section 102 of this title, if the differences between the subject matter sought to be patented and
> the prior art are such that the subject matter as a whole would have been obvious at the time the
> invention was made to a person having ordinary skill in the art to which said subject matter pertains.
> Patentability shall not be negatived by the manner in which the invention was made.

2.      Claims 1-8, 11, 15-23, 25 and 27-28 are rejected under 35 U.S.C. 103(a) as

being unpatentable over Gwon(CN 1361510) in view of  Kasai(6,989,826).

As to claims 1-8, 11, 15-23, 25 and 27-28, Gwon teaches a display panel for

image display using a voltage programming method(display an image by applying a

data voltage representing gradation)(see figure 2 and page 2, lines 9-11), the display

panel comprising a plurality of data lines(D1-Dy) for transferring a data voltage

representing an image signal, a plurality of scan lines(S1-Sz) for transferring a selection

signal, and a plurality of pixel circuits, each pixel circuit being coupled to a

corresponding the data line(e.g. D1) and two adjacent the scan lines(Sn and Sn-1),

each pixel circuit comprising: a display element capable of displaying a portion of an

image, the image portion corresponding to a quantity of applied current;  a

first transistor(M1) having a main electrode and a control electrode;  a capacitor(C1)

coupled between the main electrode and the control electrode of the first

transistor(M1), wherein the first transistor(M1) is capable of generating the applied

current in response to voltage between the main electrode and the control

electrode;  a second transistor(M2) having a control electrode coupled to the

control electrode of the first transistor(M1), the second transistor(M2) being

configured to operate as a diode;  a first switching element(M3) coupled to a main

electrode of the second transistor(M2), wherein the first switching element(M3)

transfers the data voltage from the data lines(Dm) to the second transistor(M2) in

response to the selection signal from one of the two adjacent scan lines(Sn, Sn-1), so

as to charge the capacitor(C1) with the data voltage;  a second switching element(M4)

for transferring a precharge voltage(Vpre) to the control electrode of the first

transistor(M1) in response to a first control signal(Sn-1) before the data voltage is

supplied(see figures 4, 11B, 12-15, 17 and abstract).

Gwon fails to disclose a third switch for electrically isolating the first

transistor from the display element.

Kasai teaches a display panel comprising a third switching element(213)  being

turned off in response to a second control signal(V2 is at the L level)(see figures 45(d)

and column 6, lines 32-38)  for electrically isolating a first transistor(214) from a display

element(220), so as to prevent a current being applied to the display element(220)

while the capacitor(230) is being charged with the precharge voltage(see figure 4-5(d),

19(a)-22; column 5, lines 60-68; column 6, lines 1-11 and column 16, lines 40-53).  It

would have been obvious to have modified Gwon with the teaching of Kasai, so as to

improve the display quality by individually controlling a light emitting elements and reduce power consumption(see Kasai's column 16, lines 22-31).

As to claim 2, Gwon as modified teach the third switching element(213) is coupled between the first transistor(214) and the display element(220)(see Kasai's figure 4).

As to claim 3, Gwon as modified teach the two adjacent scan Lines(Sn, Sn-1) comprise a current scan line(Sn) and a previous scan line(Sn-1), and the one of the two adjacent scan lines(Sn, Sn-1) is the current scan line(Sn)(see Gwon's figures 4 and 12).

As to claim 4, Gwon as modified teach the first control signal is the selection signal from the previous scan line(Sn-1).

As to claim 5, Gwon as modified teach the data voltage is applied to the data lines(D1-Dy) after transferring the precharge voltage(Vpre) in response to the first control signal(Sn-1) and before applying the selection signal to the current scan line(Sn)(see figures 11B,12).

As to claim 6, Gwon as modified teach the data voltage in the data lines(D1-Dy) is changed to a desired voltage before the select signal is applied to the current scan line(Sn-1).

As to claims 7 and 8, It would have been obvious to have the second control signal could be the first control signal(Sn-1) since Gwon as modified teach the third switching element is OFF when the second switching element(M4) is ON and the second switching element is PMOST and the third switching element is NMOST(see

Gwon's figure 12 and Kasai's figure 4). Therefore, the second control signal could be the first control signal so as to eliminate the control signal lines.

As to claim 11, Gwon as modified teach the third switching element is turned off during a time period of transferring the precharge voltage using the first control signal(Sn-1) and another time period of transferring the data voltage using the selection signal from the current scan line(Sn)(see Gwon's figure 12 and Kasai's figures 4, 12a-12d and 21a-21c; column 11, lines 59-68 and column 12, lines 1-5).

As to claim 15, Gwon as modified teach the first and second switching elements(M1, M2) are transistors of the same type as the first and second transistors(M3, M4, PMOST)(see figure 12).

As to claim 16, Gwon teaches the precharge voltage(ground voltage) is lower than a lowest data voltage from the data lines(D1-Dy)(see Gwon's figures 4-7; claim 10 or Corresponding US Patent No. 7015,884's figures 6-7; claim 9 and column 7, lines 20-45).

As to claim 17, Gwon as modified teaches a data driver(30) coupled to the display panel(10), the data driver(30) being capable of applying the data voltage to the data lines(D1-Dy); and a scan driver(20) coupled to the display panel(10) and scan driver(20) being capable of applying the selection signal to the scan Lines(see figure 4).

As to claims 18, 19 and 27, Gwon teaches a method for driving an image display device display using a voltage programming method(display an image by applying a data voltage representing gradation)(see figure 2 and page 2, lines 9-11) coupled to

two adjacent scan(Sn, Sn-1) lines the image display device comprising a first

transistor(M1) having a main electrode and a control electrode; a capacitor(C1)

coupled between the main electrode and the control electrode of the first

transistor(M1), the first transistor(M1) being capable of generating a current

corresponding to a voltage charged in the capacitor(C1), a second transistor(M2)

having a control electrode coupled to the control electrode of the first transistor(M1)

and being configured to operate as a diode, and a display element capable of

displaying a portion of an image corresponding to a quantity of the current generated

by the first transistor(M1), the method comprising: transferring a precharge

voltage(Vpre) to the control electrode of the first transistor(M1) in response to a first

control signal(Sn-1)during a first time period; transferring a data voltage to the control

electrode of the first transistor(M1) through the second transistor(M2) in response to a

selection signal from one of the two adjacent scan lines(Sn-1, Sn) during a second time

period; (see figures 4, 11B, 12-15, 17 and abstract).

Gwon fails to disclose a method for interrupting the transfer of data voltage and

switching means(claim 27) or first switching element(claims 29 and 30) for electrically

isolating the first transistor from a display element during at least one of the first time

period and the second time period.

Kasai teaches a display panel comprising switching means or first switching

element(213) for interrupting the  being turned off in response to a second control

signal for electrically isolating a first transistor(214) from a display element(220) during

a first time period(Tc, precharge period) of a capacitor(230) coupled to the first

transistor(214) is being charged with the precharge voltage(see figure 4-5(d), 19(a)-22; column 5, lines 60-68; column 6, lines 1-11 and column 16, lines 40-53). It would have been obvious to have modified Gwon with the teaching of Kasai, so as to improve the display quality by individually controlling a light emitting elements and reduce power consumption(see Kasai's column 16, lines 22-31).

As to claim 20, Gwon as modified teach the two adjacent scan lines(Sn, Sn-1) comprise a current scan line(Sn) and a previous scan line(Sn-1), and the one of the two adjacent scan lines(Sn, Sn-1) is the current scan line(Sn)(see Gwon's figures 4 and 12).

As to claims 21 and 28, Gwon as modified teach the first control signal is the selection signal from the previous scan line(Sn-1).

As to claim 22, Gwon as modified teach the first transistor(M1) is electrically isolated from the display element(OLED) in response to the selection signal from the previous scan line(Sn-1) during the second time period(transferring data voltage period)(see Gwon's figure 12 and Kasai's figure 4, 21a-21c and column 16, lines 32-39).

As to claim 23, Gwon as modified teach the first transistor(M1) is electrically isolated from the display element(OLED) in response to a second control signal(V2) during the second time period(transferring data voltage period)(see Gwon's figure 12 and Kasai's figure 4, 21a-21c and column 16, lines 32-39).

As to claim 25, Gwon as modified teach a method for preventing the precharge voltage(Vpre) and the data voltage from being transferred to the control electrode of

the first transistor(M1) between the first and second time periods(precharging period

and transferring data voltage period)( see Gwon's figure 12 and Kasai's figure 4, 21a-

21c and column 16, lines 32-39).

## Allowable Subject Matter

3.     Claims 9-10, 12-14, 24, 26,  31-34 and 36-37 are  allowable.

## Response to Arguments

4.     Applicant's arguments with respect to claims 1-8, 11, 15-23, 25 and 27-28 are

have been considered but are moot in view of the new ground(s) of rejection.

Applicants argue that Kasai teach a current programming type display device on

page 15.  However, Gwon teaches a voltage programming type display device(display

an image by applying a data voltage representing gradation)(see figure 2 and page 2,

lines 9-11).

Applicants argue that the storage capacitor(230) of Kasai holds an electric

charge corresponding to a current of the data signal on page 15.  However,  Gwon

teaches a storage capacitor(C) holds an electric charge corresponding to a voltage of

the data signal(see figure 2 and page 2, lines 9-11) and Kasai teaches the storage

capacitor(230) can hold a voltage(see figure 4 and column 6, lines 47-49).

In response to applicant's argument that there is no suggestion to combine the

references on page 16, the examiner recognizes that obviousness can only be

established by combining or modifying the teachings of the prior art to produce the

claimed invention where there is some teaching, suggestion, or motivation to do so

found either in the references themselves or in the knowledge generally available to one

of ordinary skill in the art.  See *In re Fine*, 837 F.2d 1071, 5 USPQ2d 1596 (Fed. Cir.

1988)and *In re Jones*, 958 F.2d 347, 21 USPQ2d 1941 (Fed. Cir. 1992).  In this case,

Gwon and Kasai both teach an EL display device and the motivation to combine these

two references has been found in  the references themselves or in the knowledge

generally available to one of ordinary skill in the art(see paragraph #2 above).


### *Conclusion*


**THIS ACTION IS MADE FINAL.**  Applicant is reminded of the extension of time

policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE

MONTHS from the mailing date of this action.  In the event a first reply is filed within

TWO MONTHS of the mailing date of this final action and the advisory action is not

mailed until after the end of the THREE-MONTH shortened statutory period, then the

shortened statutory period will expire on the date the advisory action is mailed, and any

extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of
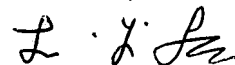
the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

5.      Any inquiry concerning this communication or earlier communications from the examiner should be directed to Lun-yi Lao whose telephone number is 571-272-7671. The examiner can normally be reached on M-F.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Bipin Shalwala can be reached on 571-272-7681. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

June 6, 2007

**Lun-yi Lao**
**Primary Examine**